Semiconductor Devices and Circuits:

Smaller, faster, denser and what it all means.

SEMI-THERM XV

Evening Tutorial

March 9, 1999

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National Institute of Standards and Technology

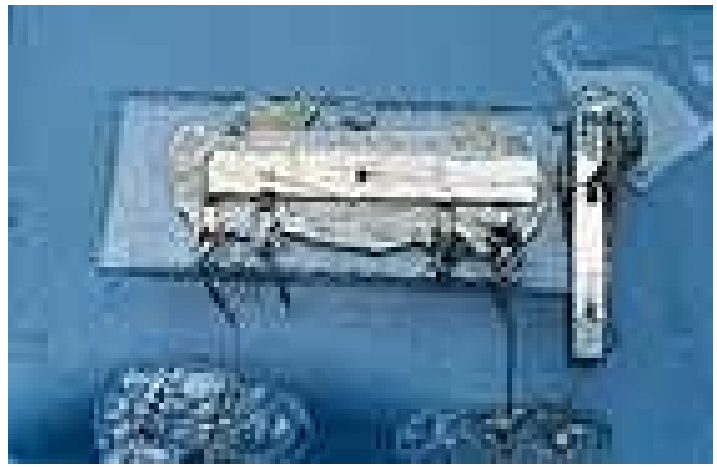
Gaithersburg, MD

+**Currently at the Semiconductor Research Corporation**

Research Triangle Park, NC

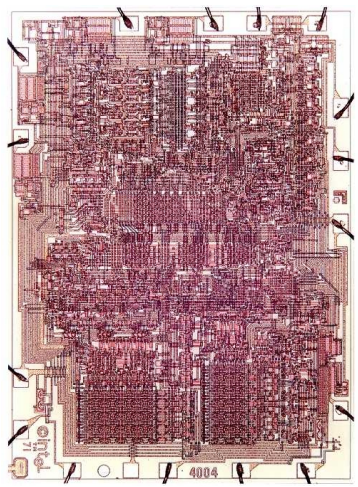
The Starting Point

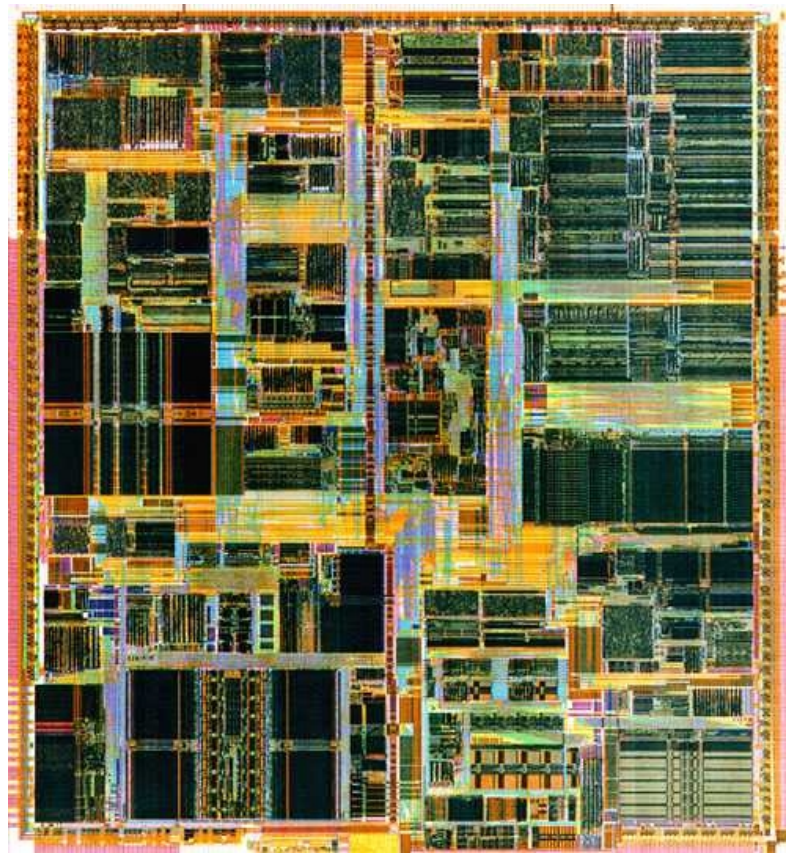
First Transistor
Bell Labs, 1947
www.lucent.com



First Integrated Circuit
Texas Instruments, 1958
www.ti.com

Yesterday and Today



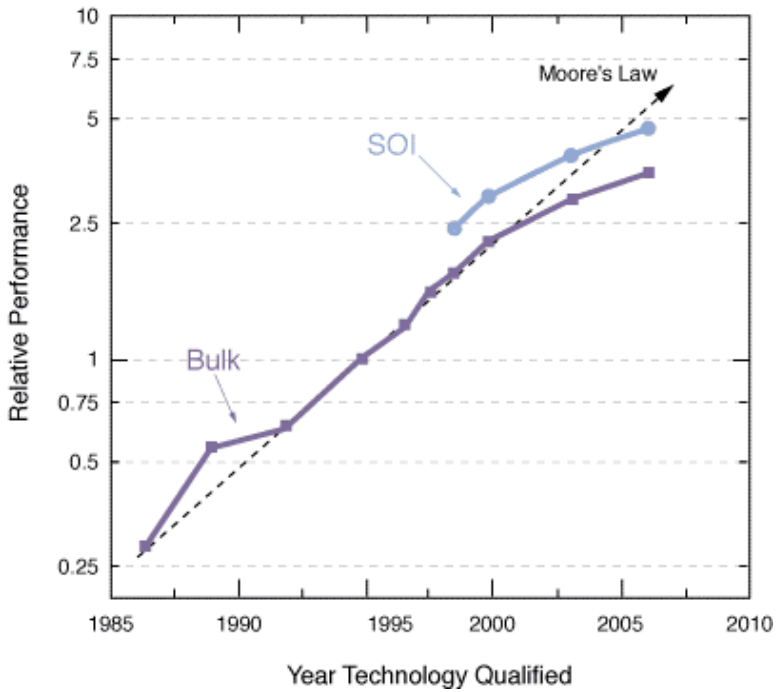


Intel 4004-2.3x10^3 transistors
1970

Intel Pentium II-7.5x10^6 transistors
Today

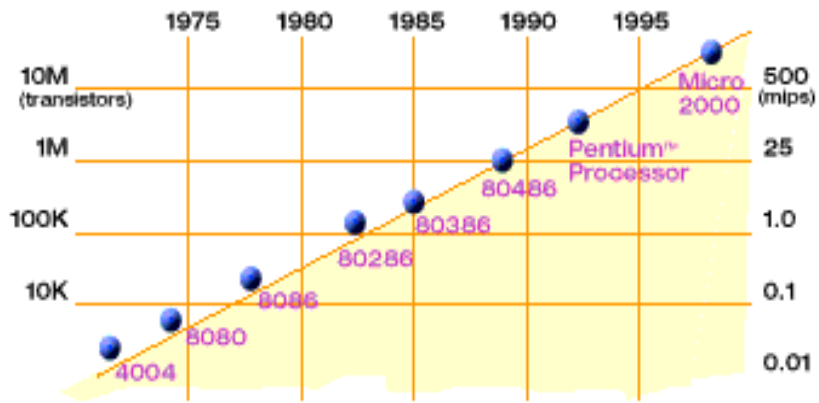
www.intel.com

The Imperative



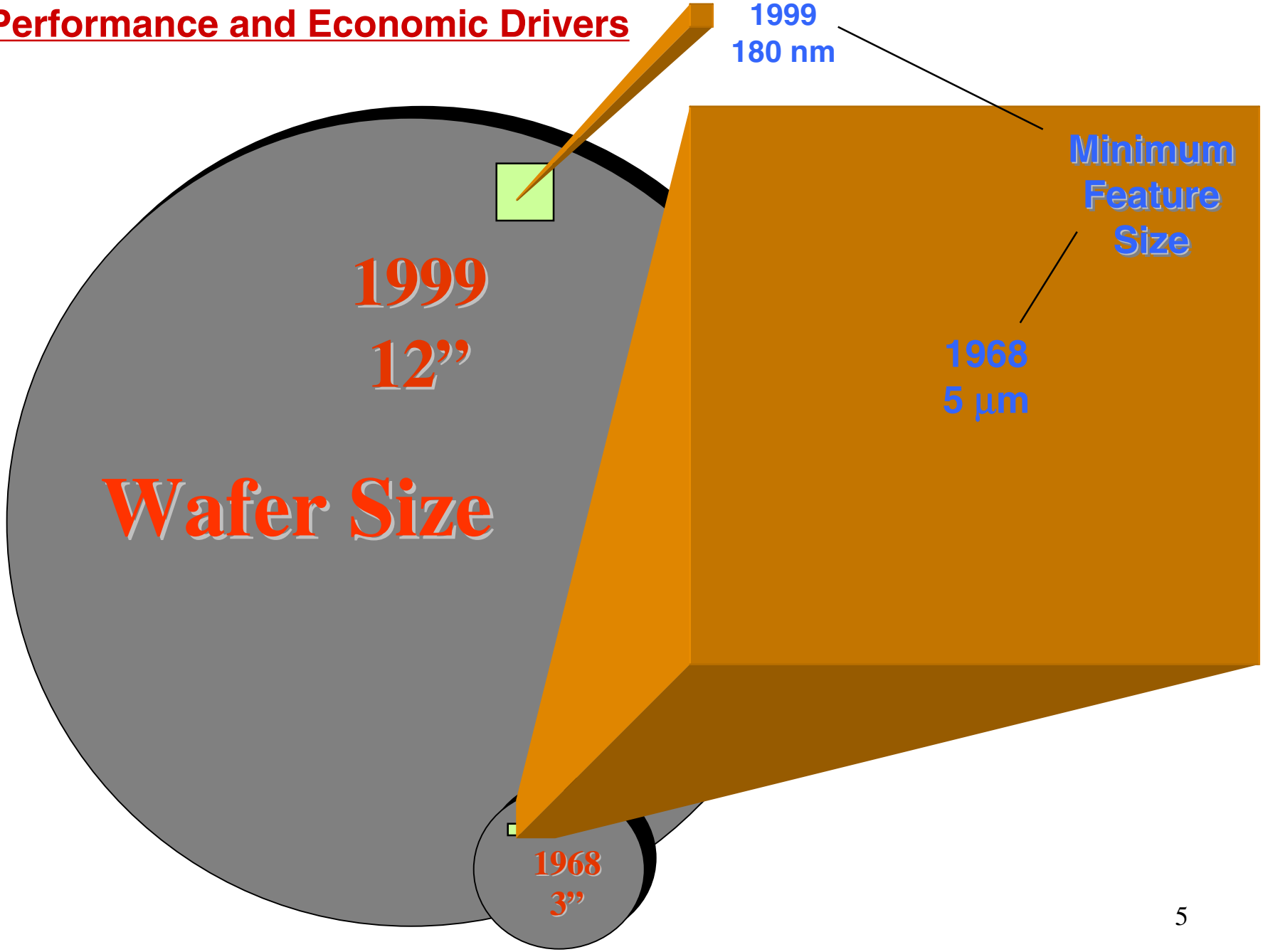
www.ibm.com

Moores Law: Performance doubles with every new chip generation (approximately every 18-24 months)-- observed by Gordon Moore in 1965.



www.intel.com

Performance and Economic Drivers



National Technology Roadmap for Semiconductors (NTRS)

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Technology Generations Isolated Lines (1/2 pitch) (nm)	250	180	150	130	100	70	50
Logic Transistors/cm^2	3.7M	6.2M	10M	18M	39M	84M	180M
Chip Frequency (on-chip clock) (MHz)	750	1250	1500	2100	3500	6000	10000
Chip size (mm^2)	280	400	445	560	790	1120	1580
Power Supply Voltage (V)	2.5-1.8	1.8-1.5	1.5-1.2	1.5-1.2	1.2-0.9	0.9-0.6	0.6-0.5
Maximum Power (V) High Performance	70	90	110	130	160	170	175
Maximum Power (V) Hand Held	1.2	1.4	1.7	2	2.4	2.8	3.2
Chip IO's	1450	2000	2400	3000	4000	5400	7300
T_J/T_A (C)	125/55	125/55	125/55	125/55	125/55	125/55	125/55

Definition of SEMICONDUCTOR:

A material that has an electrical resistance between that of an electrical insulator (e.g., glass/SiO_2) and an electrical conductor (e.g., Cu)!

Examples: Ge, Si, GaAs, SiGe, SiC, ...

Why Semiconductors?

- The electrical conductivity (the reciprocal of the resistivity) can be varied by intentionally adding specific impurities (dopant) to the semiconductor.
- Two types of particles carry electrical current in a semiconductor, negatively charged electrons (n) and positively charged holes (p).

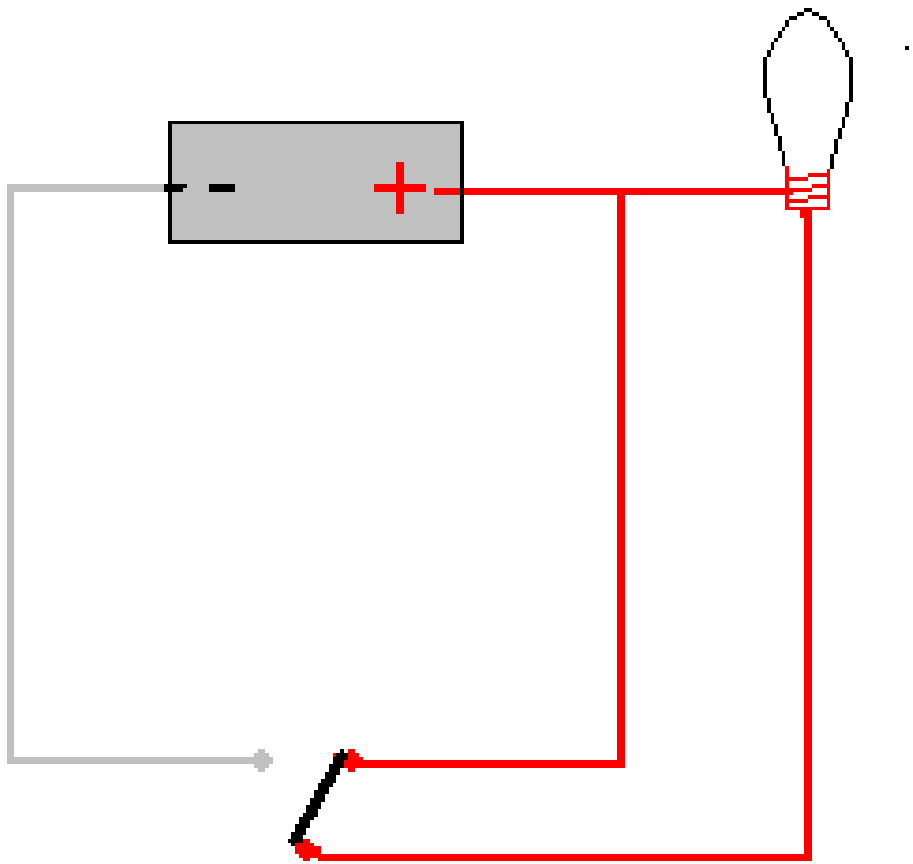
Why Silicon?

- An oxide (SiO_2) that is electrically, mechanically, and chemically stable readily forms on the surface of Si.
- Today, a tremendous technological base and infrastructure exists for the manufacture of Si integrated circuits.

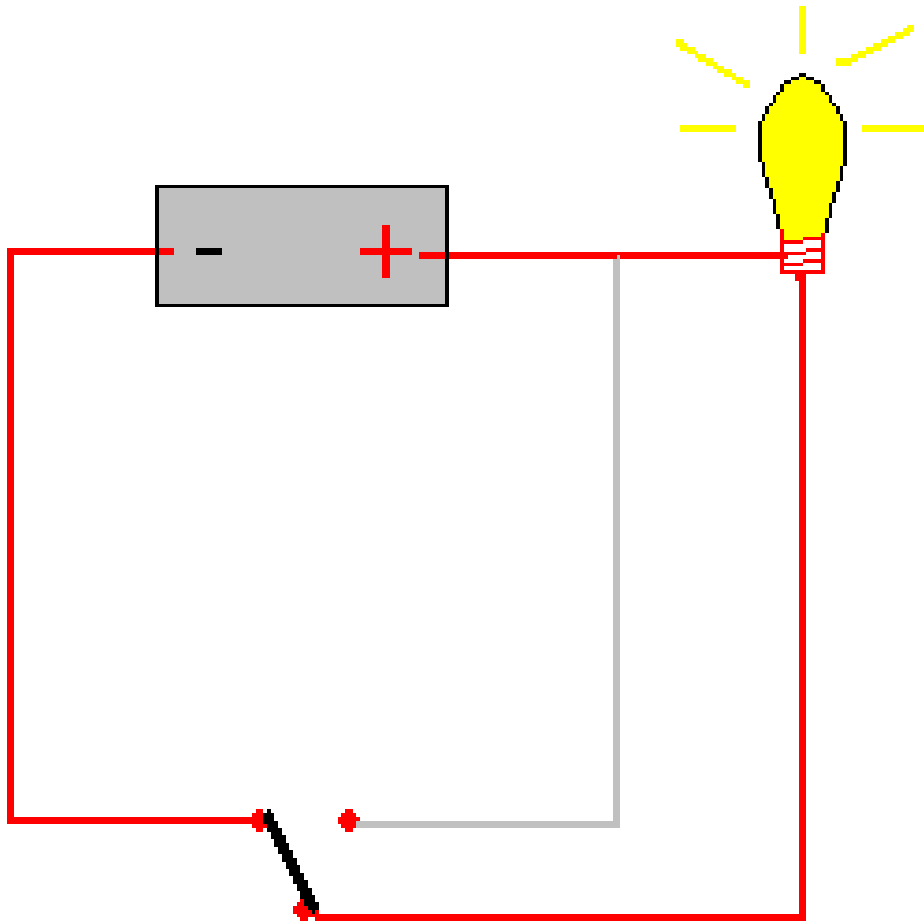
What is a Transistor?

- A transistor is an electronic component that has 3 terminals.
- Applying a small signal to 1 of the terminals (gate of a MOSFET/base of a bipolar) allows a large current to flow between the other 2 terminals (source-drain of a MOSFET/emitter-collector of a bipolar).
  - **Thus, the transistor is an electronic amplifier (the small signal is amplified) and,**
  - **The transistor is an electronic switch (the presence of the small signal allows a large current to flow, the absence of the small signal at the gate/base, allows NO current to flow.**

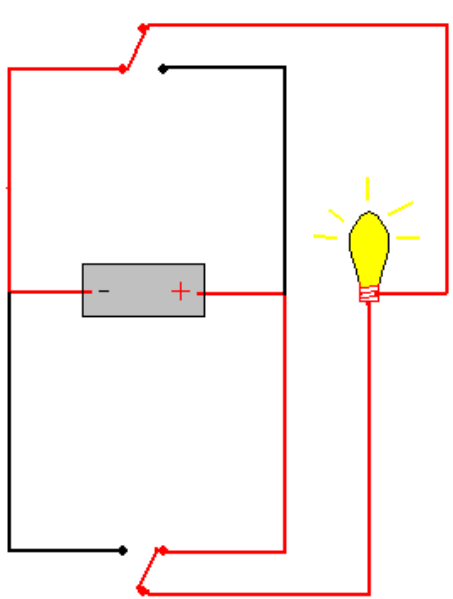
A 'Macro' Switch



A 'Macro' Switch



A ‘Macro’ Switch
3-way



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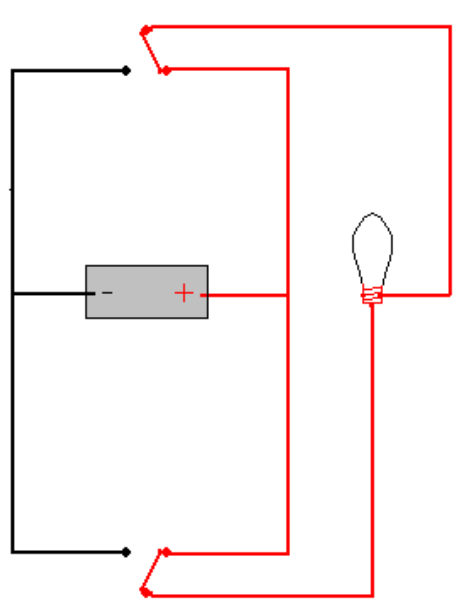

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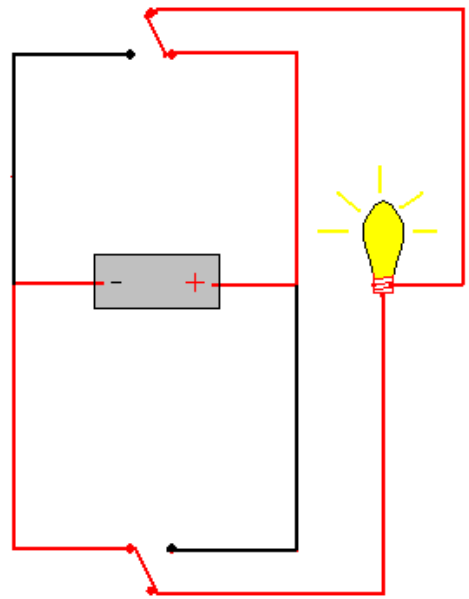


1

Characteristics of a Good Switch

- Very low resistance when ‘on’.
- Very large resistance when ‘off’.
- Requires very little energy to switch from on to off and vice versa.
- Can be switched very rapidly.
- Is inexpensive to manufacture.
- Can be integrated with other switches and components into a very small volume.

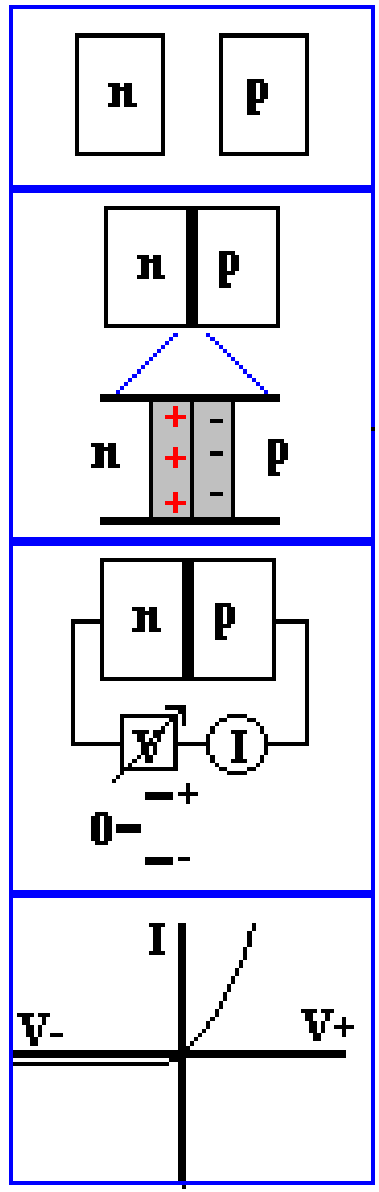
Just the Basics

Doping makes the Si n-type (electrons) or p-type (holes).

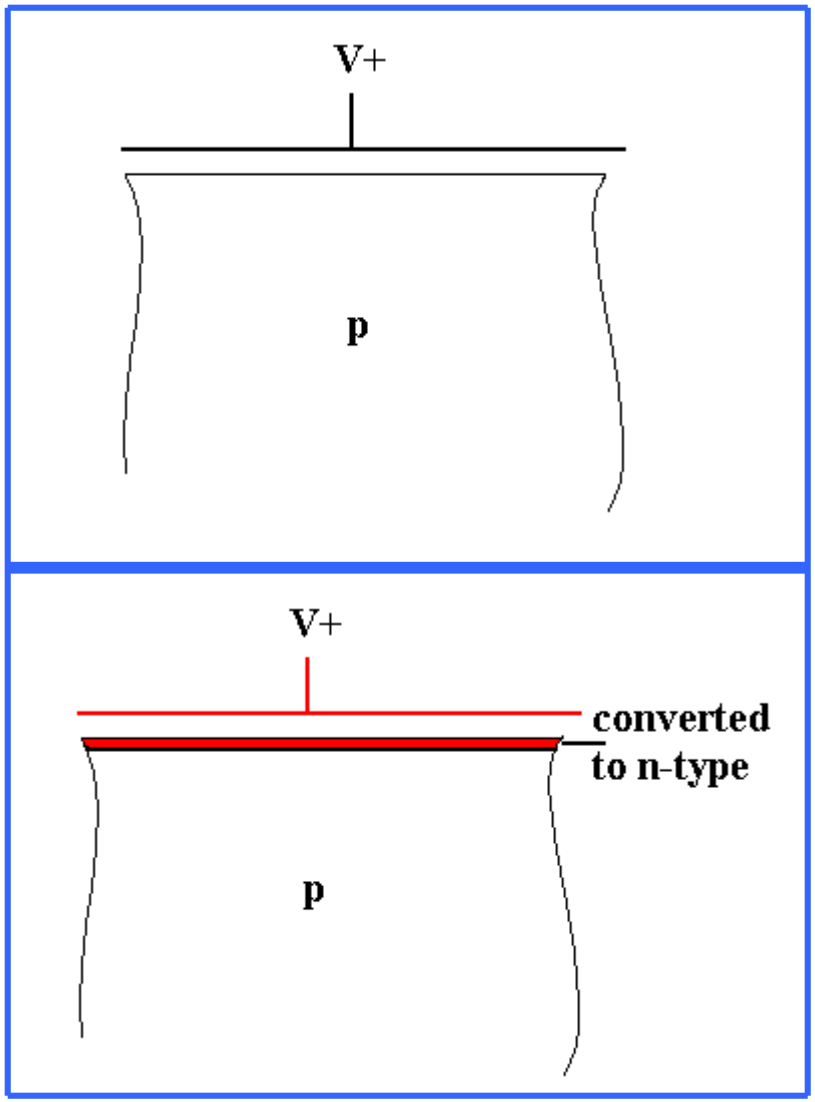
Brought together, a pn junction is formed. Initially, electrons flow to the p-type side and holes flow to the n-type side. An 'electric dipole' is formed that stops the flow. No current flows at equillibrium.

Applying a voltage to either side of the junction, either opposes the 'dipole' allowing current to flow (forward bias) or reenforces the 'dipole' keeping current from flowing (reverse bias)

For forward bias, a large current can flow through the junction. For reverse bias, no (or very small) current can flow.



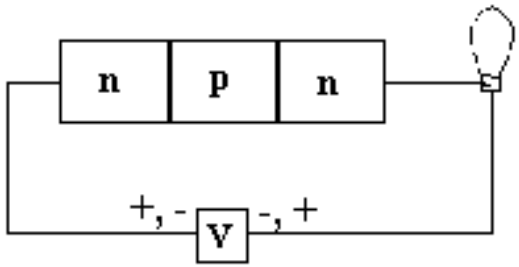
Just the Basics (cont.)



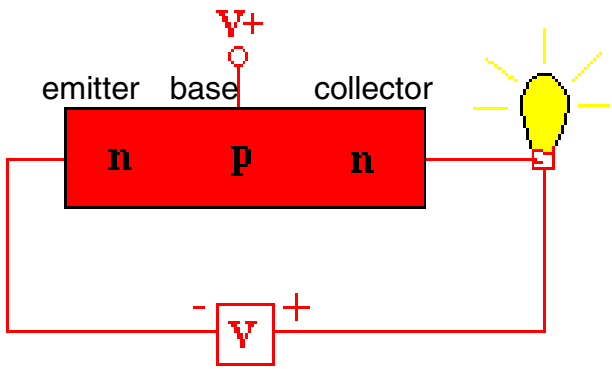
A capacitor can be made by bringing a metal plate close to the surface of a semiconductor. The space between the plate and the semiconductor is filled with a dielectric, such as SiO_2.

By applying a voltage to the plate, electric charge is attracted to the surface. In the example here, the positive voltage attracts electrons and the surface is 'inverted' to n-type (the semiconductor bulk is p-type where holes are the carriers of electric current.)

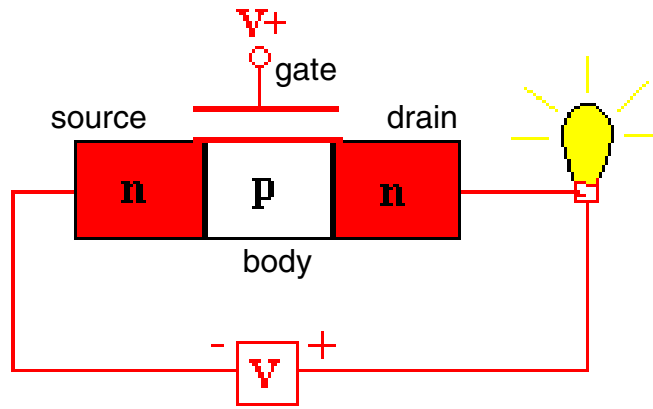
Transistor Action



A transistor consists of an n-p-n (or p-n-p) structure. The ‘p’ region above isolates the n regions from each other.



A ‘bipolar’ transistor has a direct electrical attachment to its ‘base’. This can be used to electrically connect the n-regions above.



A MOSFET transistor has a capacitive contact to its ‘body’ region. This can be used to make the surface of that region electrically conductive, connecting the n regions together. The MOSFET transistor requires less power to operate than a bipolar. It is the transistor of choice, except for very specialized applications.

Some Definitions

Bipolar

Refers to the fact that both electrons and holes are important to the conduction of current through the device.

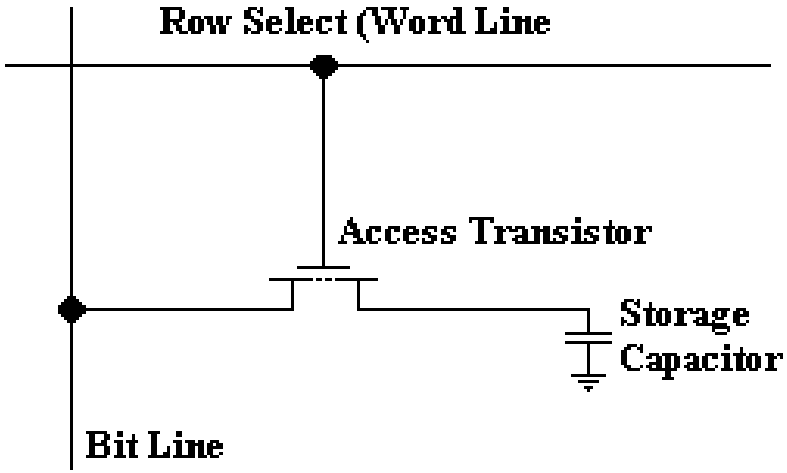
MOSFET

Metal Oxide Semiconductor Field Effect Transistor. The gate of a MOSFET is composed of a metal-oxide-semiconductor capacitor. The transistor conducts current because of the effect of the electric field at the surface of the body.

CMOS

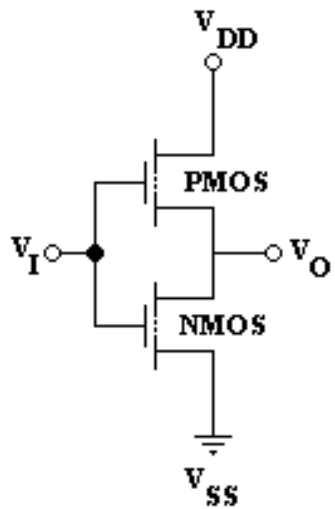
Complimentary MOS. The chip includes both p-channel and n-channel MOS transistors.

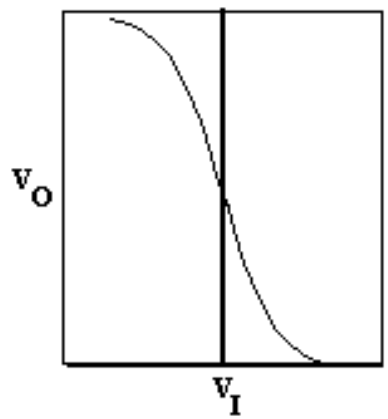
‘Micro’ Switches



DRAM Cell

CMOS Inverter



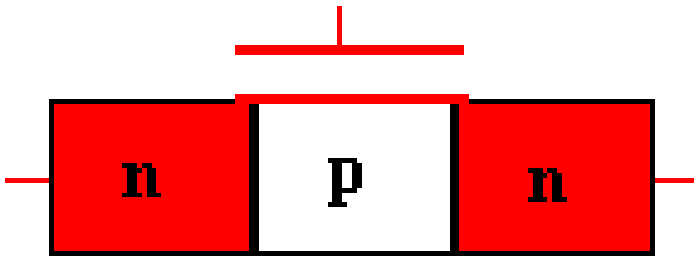


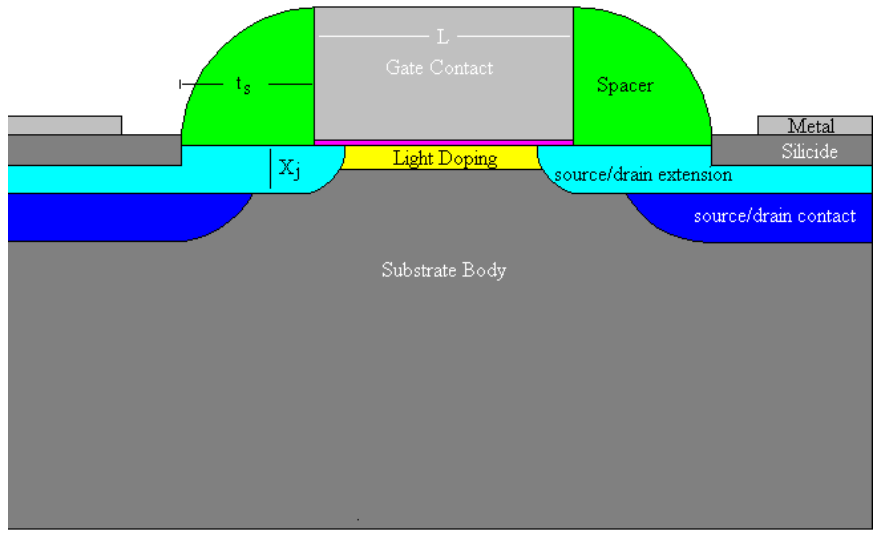
It's

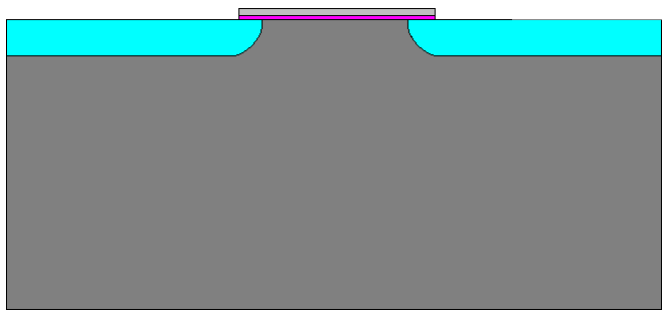
the MOSFET,

stupid!

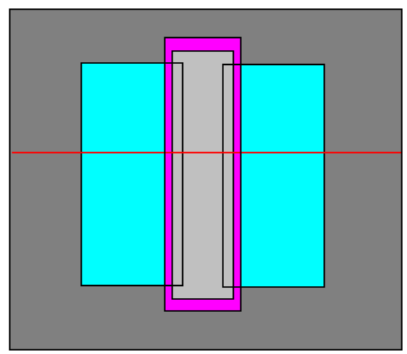
Stages of Conceptualization







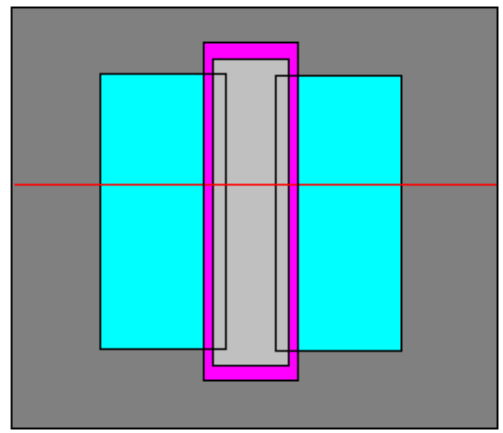
Cross-section

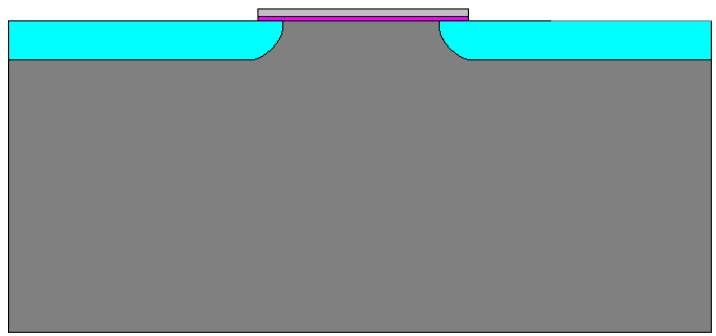


Top View

Shrinking the MOSFET and Constant Electric Field Scaling

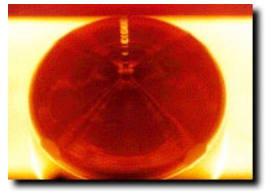
- If scaling factor is S (S>1), then:
  - Lateral feature dimensions-1/S
  - Vertical dimensions-1/S
  - Impurity concentrations-S
  - Currents and voltages-1/S
  - Current density (A/μm)-1
  - Capacitance/Area-S
  - Delay time-1/S
  - Power dissipation-$1/S^2$
  - Power density-1
- For NTRS nodes, $S=\sqrt{2}$

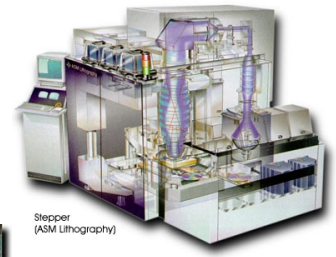




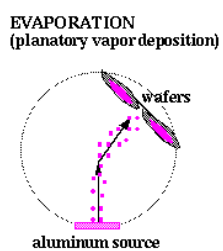
Semiconductor Processing Steps

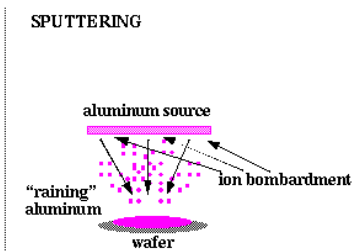
- **Starting Material**
  - Grow Ingots
  - Cut Wafers
- **Lithography**
  - Optical (UV, DUV,EUV)
  - e-beam, X-ray
- **Impurity Doping**
  - Implantation
  - Annealing, Diffusion
- **Thin Film Growth (Oxidation)**
- **Thin Film Deposition**
  - Metals
  - Dielectrics
  - Planarization

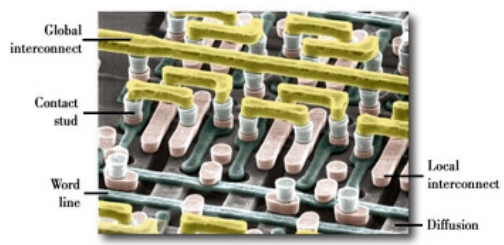

Inside CZ Puller
(MEMC)


Stepper
(ASM Lithography)


Oxidation Furnace
(Silicon Valley Group - Thermco Systems)







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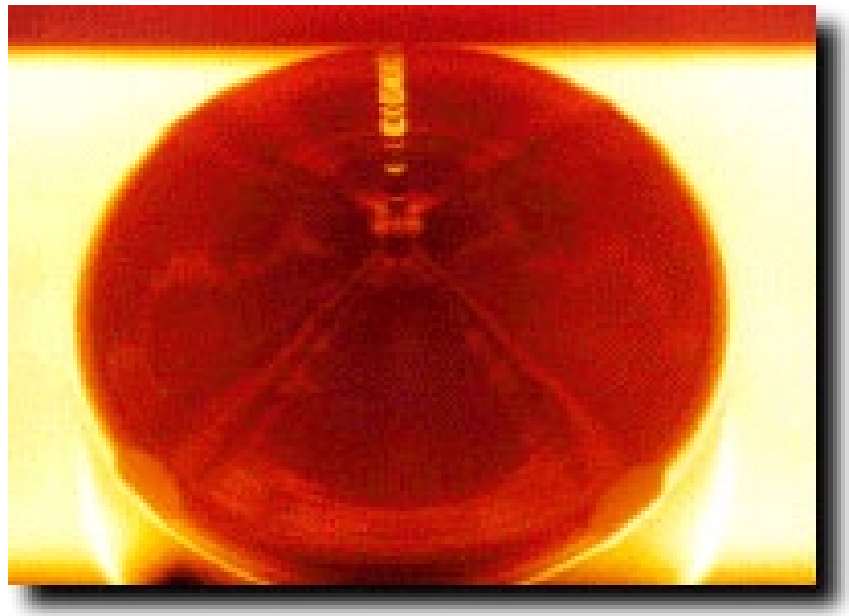
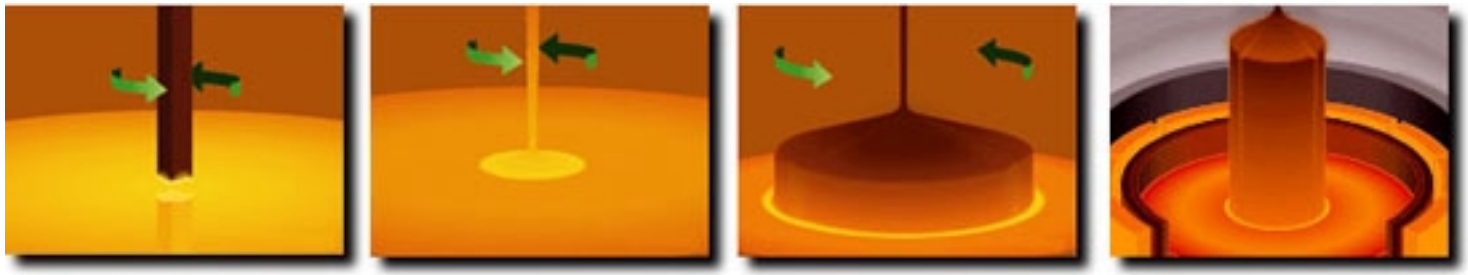
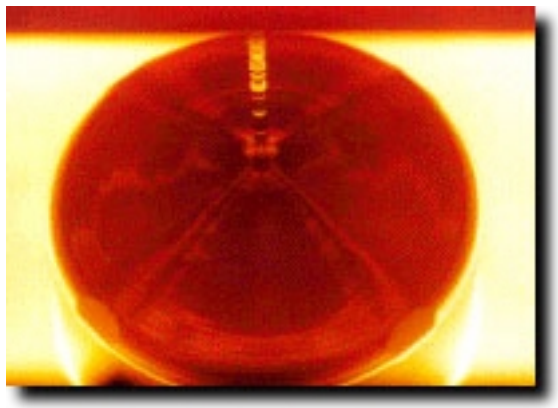


Inside CZ Puller
(MEMC)

Growing Silicon Ingots





Inside CZ Puller
(MEMC)

CZ Crystal Pullers
(Mitsubishi Materials Silicon)

Single Crystal Silicon Ingot

www.fullman.com

Starting Si Wafers

Facts

- 8“ (200 mm) diameter
  - 12” (300 mm) soon.
- Cut from ingots grown from a melt.
- Most pure and perfect material known.
  - ~1 unintentional impurity per 10^{11} Si atoms.
  - Crystal perfection over cm. distances.
- Polished mirror-like on side to be processed.
- Particle-free surface.
  - 0 particles > 100nm, less than 100 particles as large as that.
  - must be maintained throughout all of the processing.
- Flat.
  - <200 nm variation over a 2.5 cm. X 2.5 cm area.

ID Wafer Slicing Saw

Semiconductor Processing Steps

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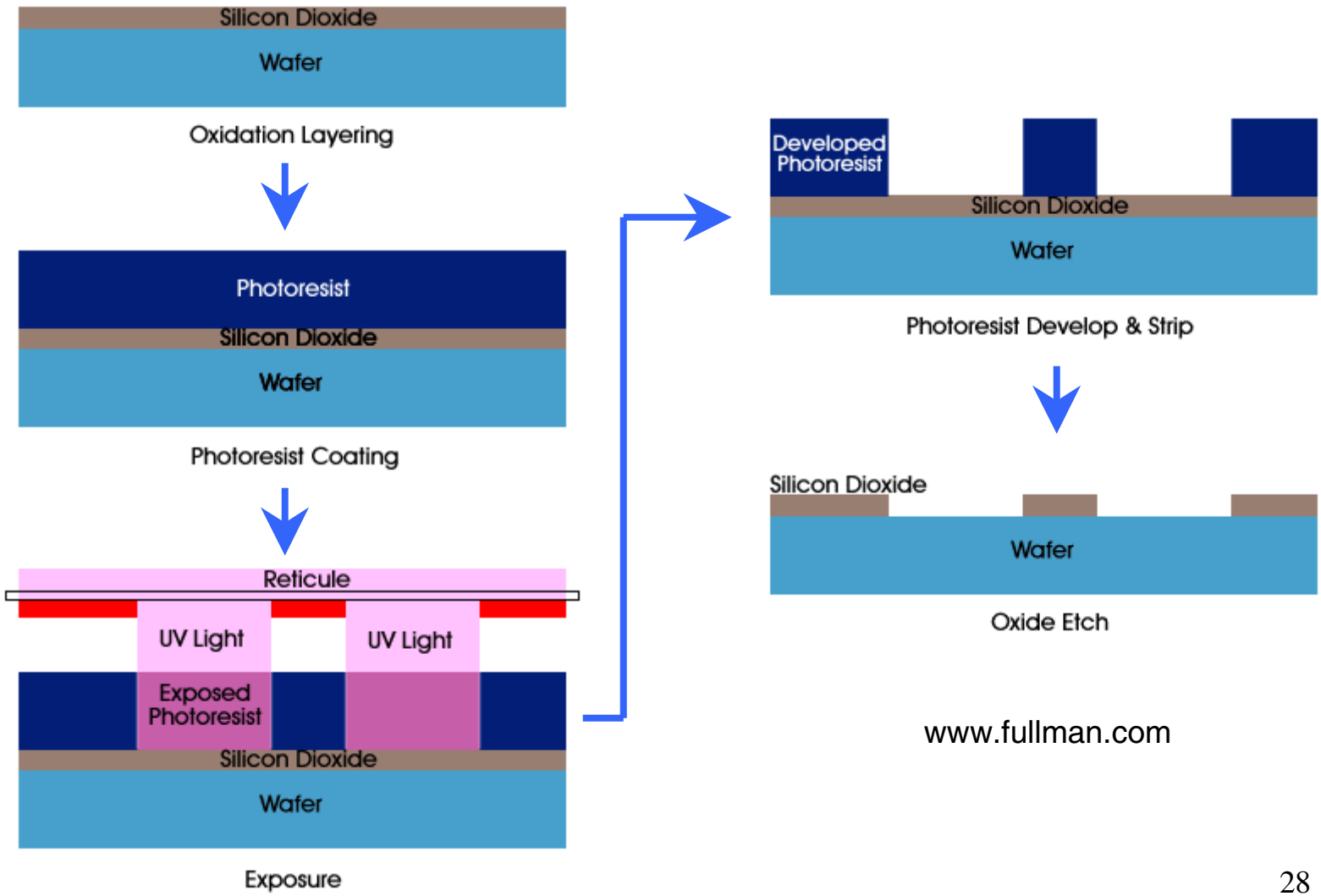
Stepper
(ASM Lithography)

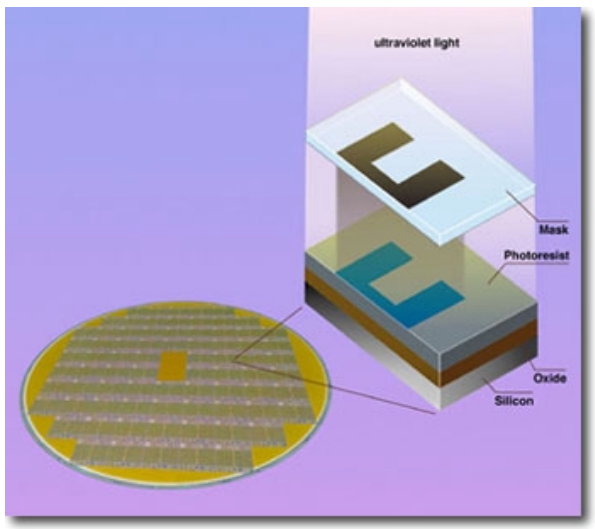
Lithography

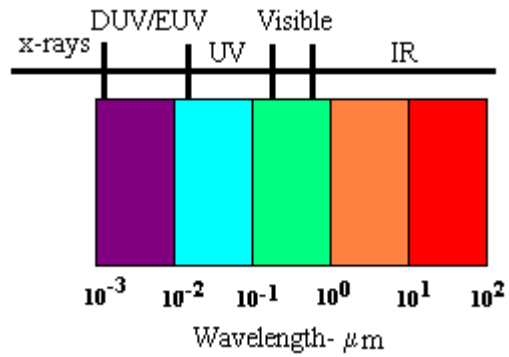


www.fullman.com

Litho Requirements

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Technology Generations Isolated Lines (1/2 pitch) (nm)	250	180	150	130	100	70	50
Exposure Technology	248 nm DUV	193 nm DUV	X-Ray	EUV	E-beam Projection	E-beam Direct Write	Ion Projection
Image Placement (nm)	52	36	32	28	20	16	12
CD Uniformity (nm)	26	18	16	13	9	6	4





New Technologies introduced every generation?

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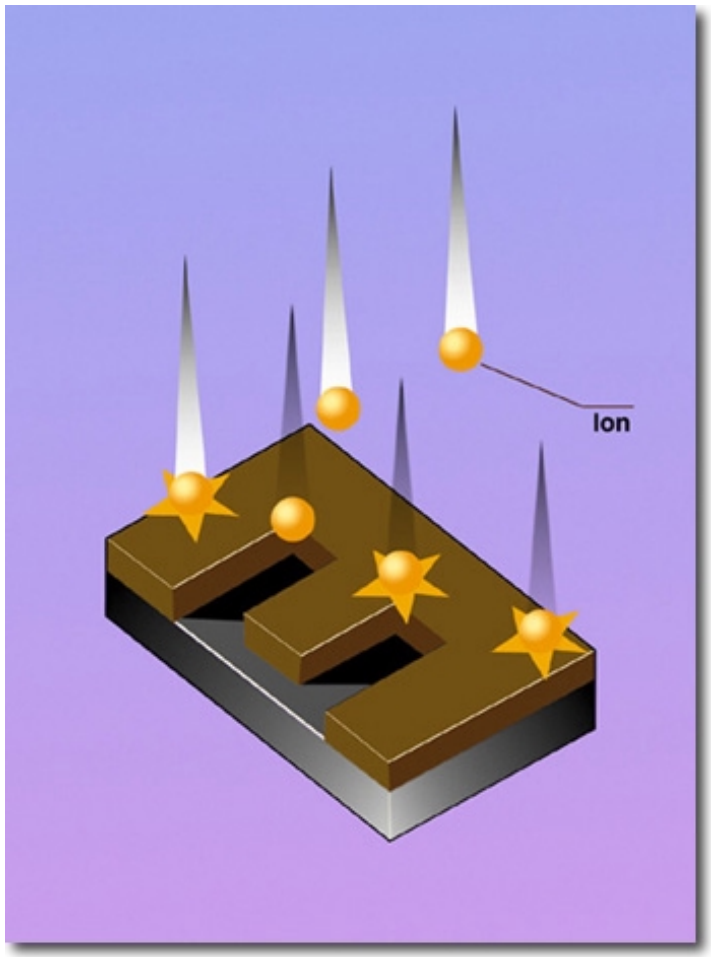
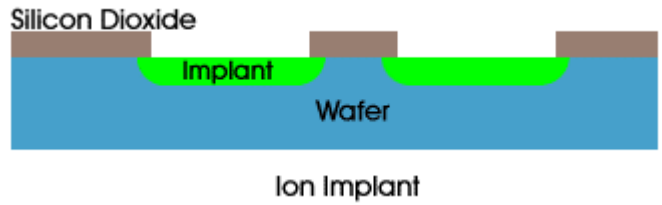
Introduction of Impurities

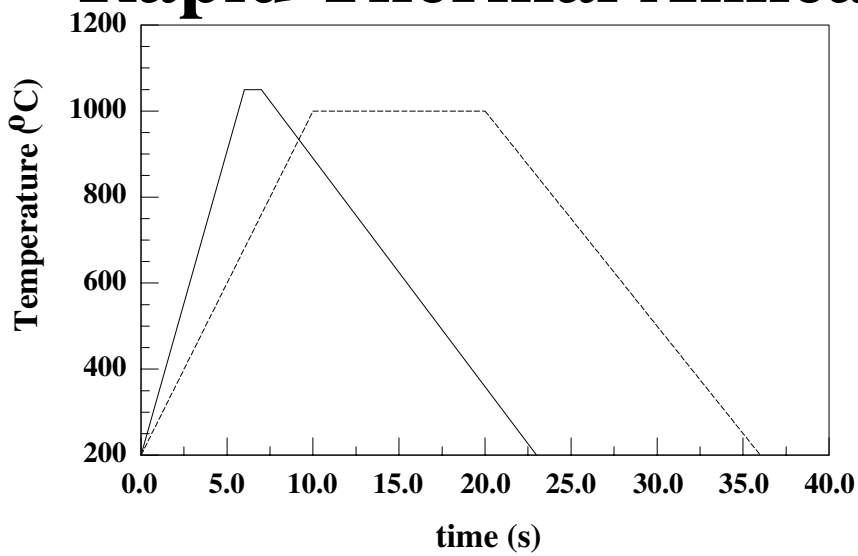


Ion Implantation



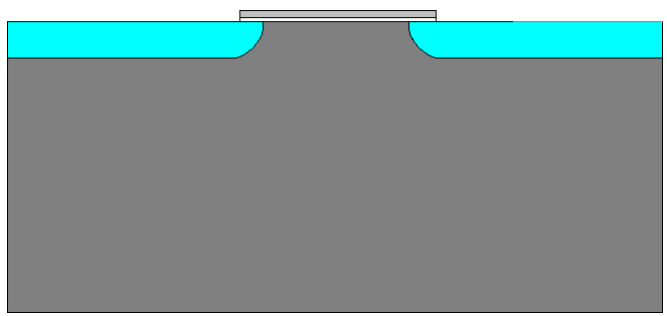
Ion Implant

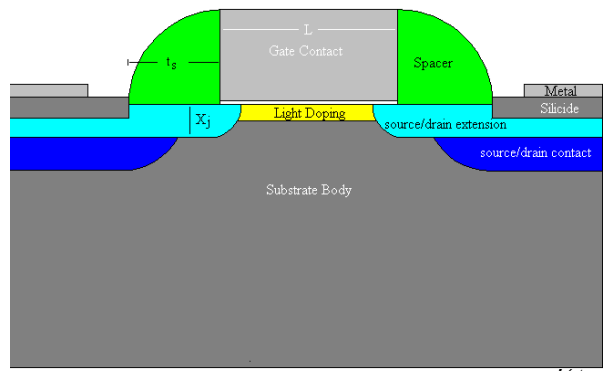
Rapid Thermal Annea



Doping Technology Requirements

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Technology Generations Isolated Lines (1/2 pitch) (nm)	250	180	150	130	100	70	50
Drain/Source Structure	Drin Extension				Elevated S/D	Elevated Single S/D	
Junction Depth at Channel (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20
S/D Extension Concentration (cm^{-3})	$1x10^{18}$	$1x10^{19}$	$1x10^{19}$	$1x10^{19}$	$1x10^{20}$	$1x10^{20}$	$1x10^{20}$





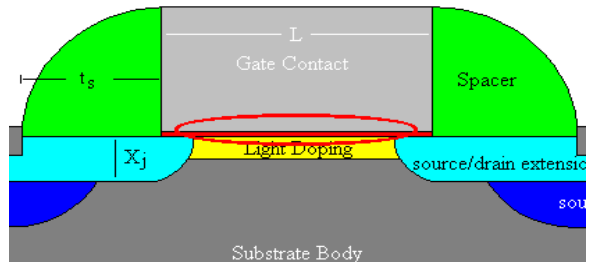
Semiconductor Processing Steps

- Starting Material
  - Grow Ingots
  - Cut Wafers
- Lithography
  - Optical (UV, DUV,EUV)
  - e-beam, X-ray
- Impurity Doping
  - Implantation
  - Annealing, Diffusion
- **Thin Film Growth (Oxidation)**
- Thin Film Deposition
  - Metals
  - Dielectrics
  - Planarization

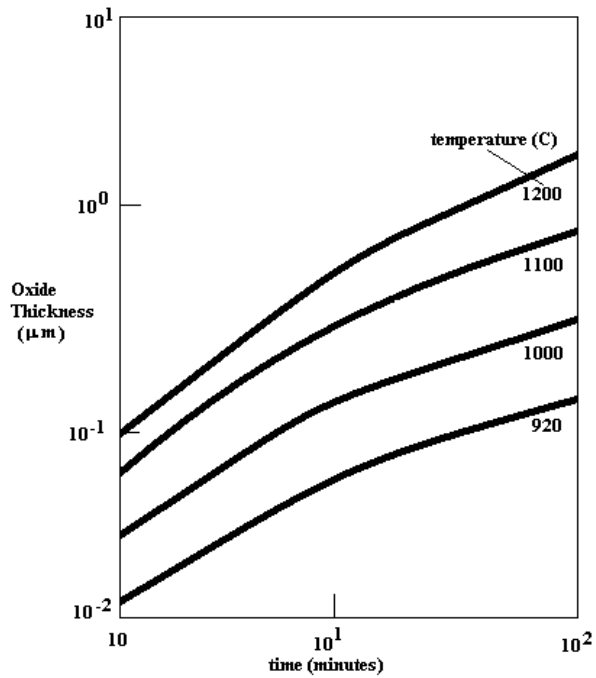
Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

Gate Stack

Year of first product shipment	1997	1999	2001	2003	2006	2009	2012
Technology Generations Isolated Lines (1/2 pitch) (nm)	250	180	150	130	100	70	50
Tox Equivalent Thickness (nm)	4--5	3--4	2--3	2--3	1.5--2	<1.5	<1.0



- Gate-Channel C/A ($k_{ox}\varepsilon_0/t_{ox}$) scales as S.
- Gate leakage current due to tunneling likely to be too large at t_{ox}<1.5 nm.
- Search for alternate gate dielectrics:
  - higher k than SiO_2
  - lower leakage for equivalent thickness
  - good interface with Si
  - compatible with all other processes.



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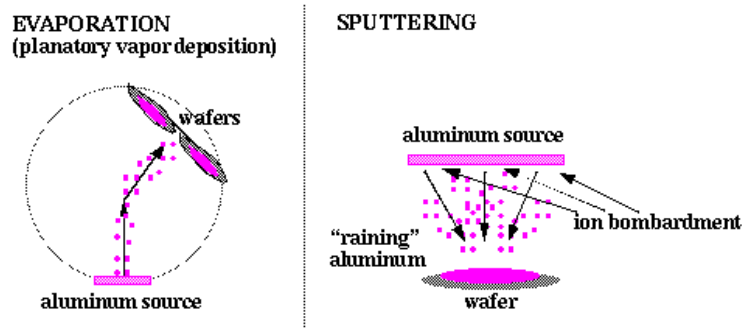
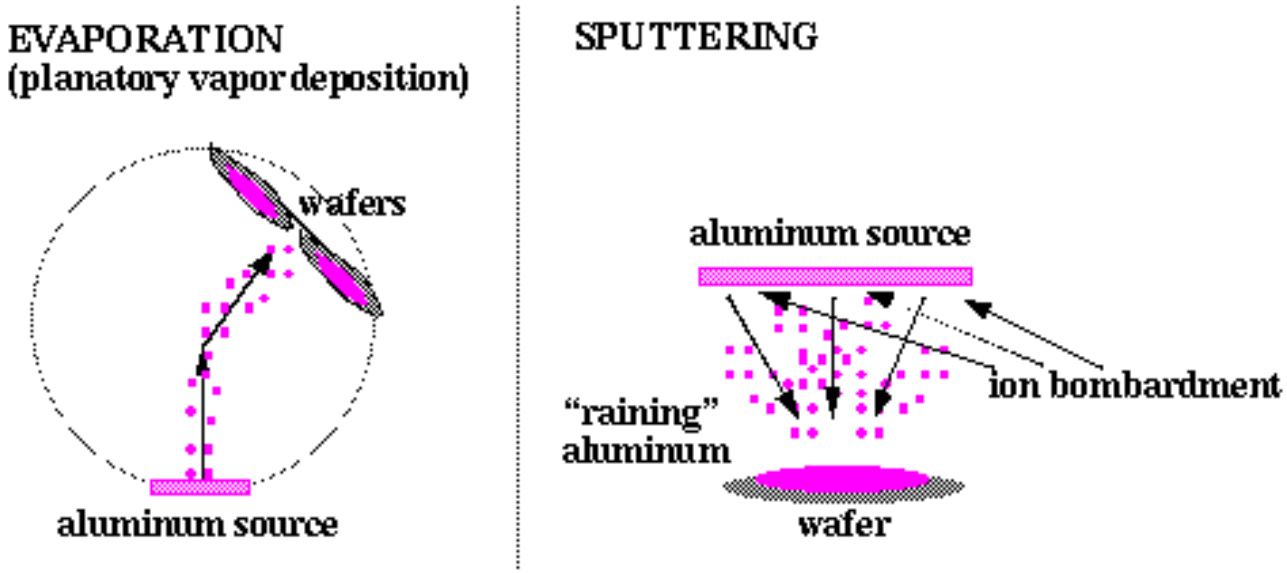
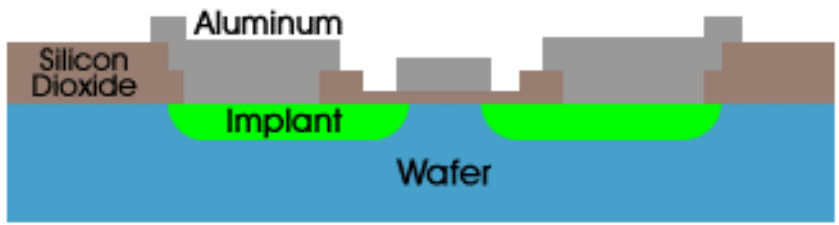


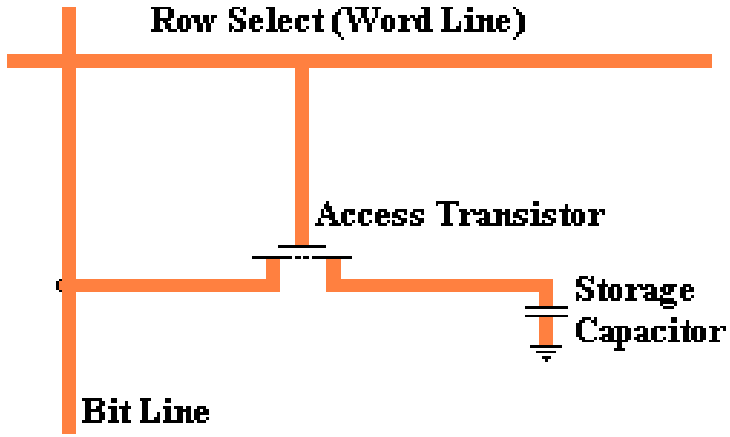
Metalization

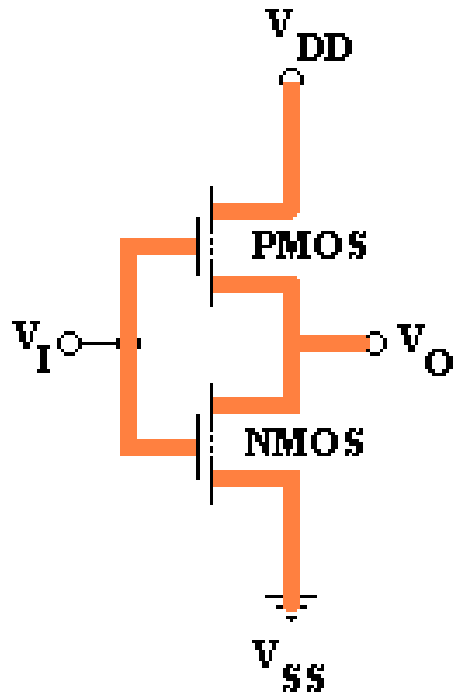


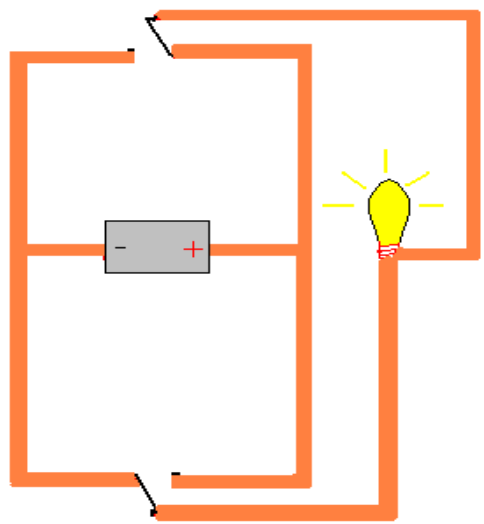


Metal Deposition

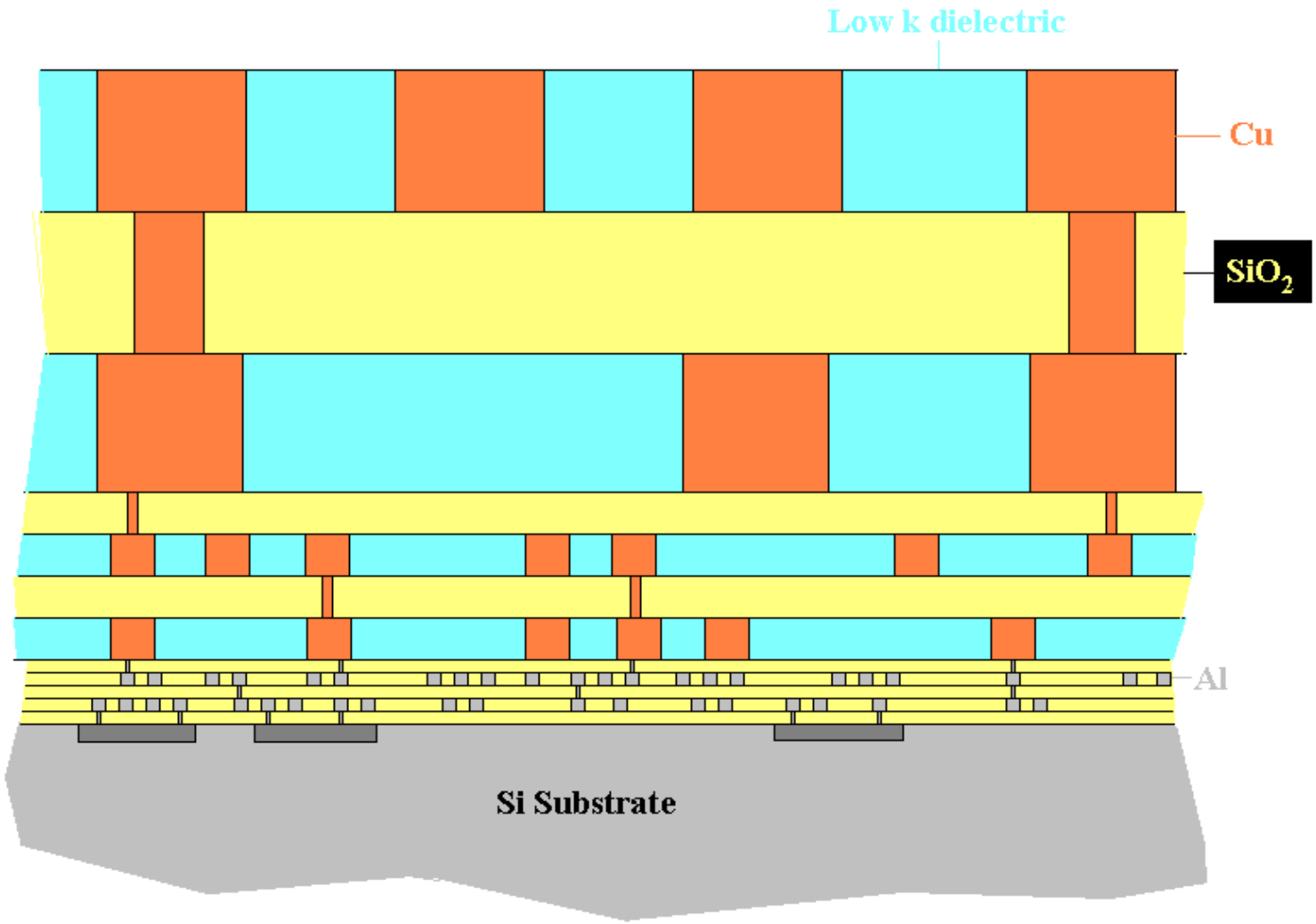
Interconnects



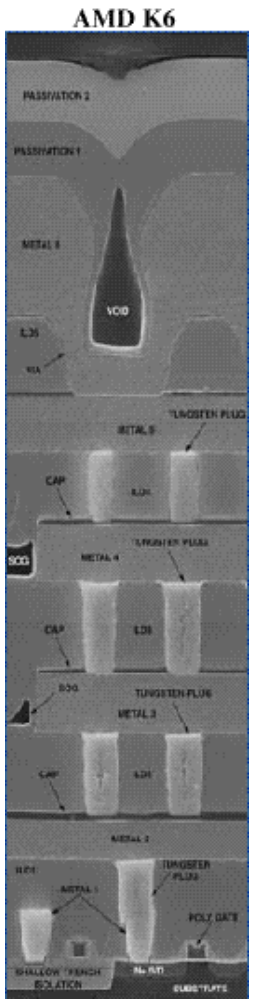


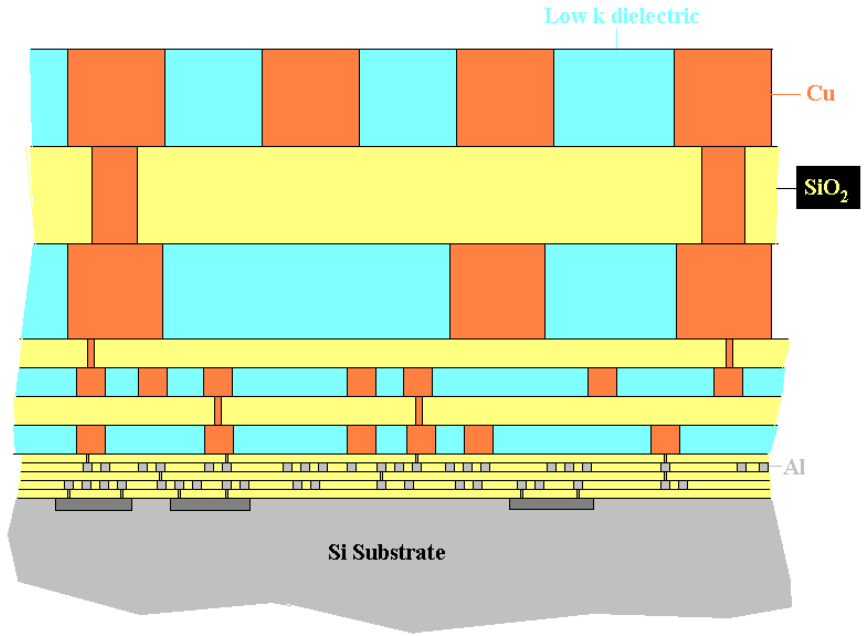


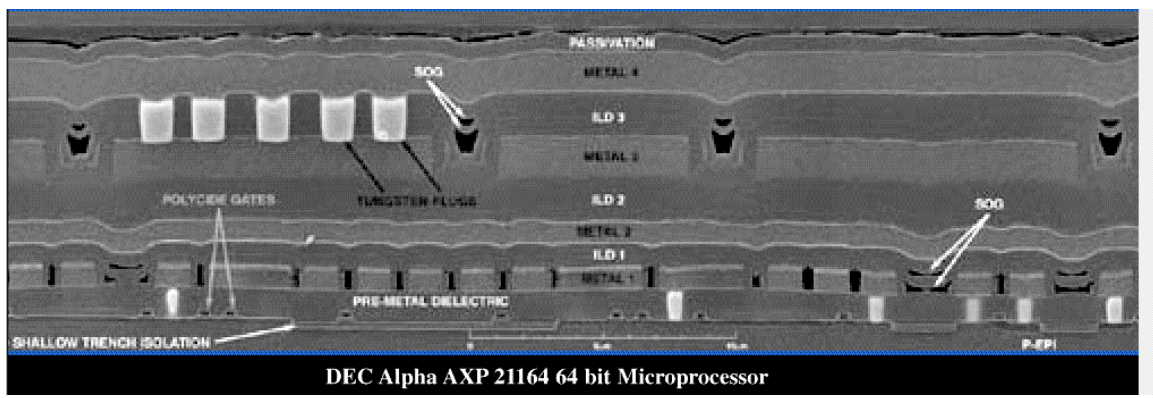
IC Interconnects



Chip Cross-sections





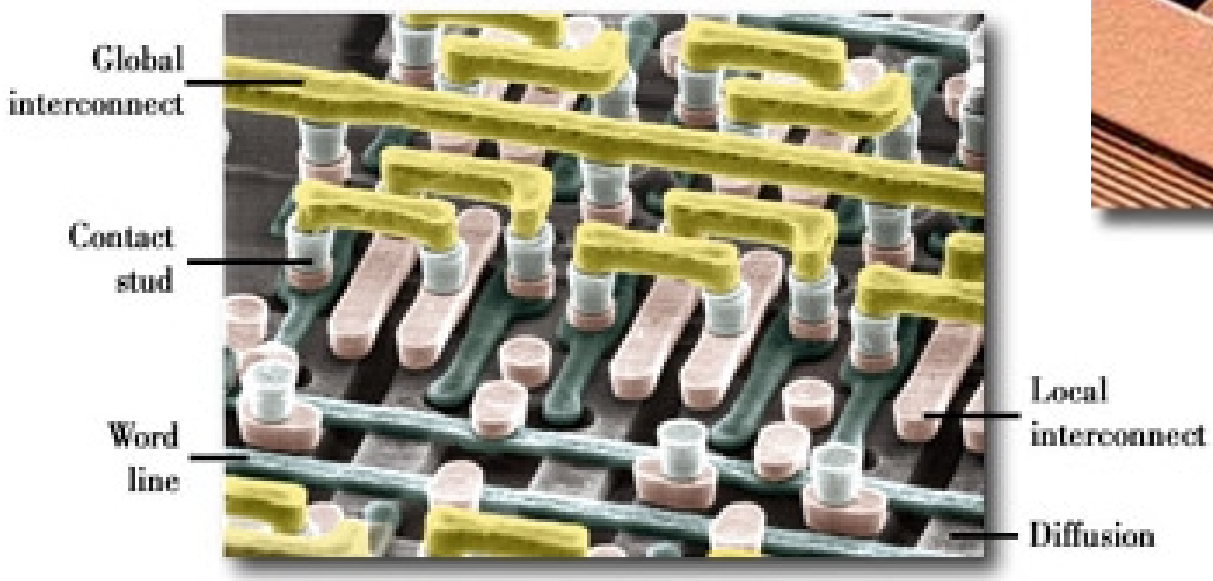


Interconnects

Example of Cu Interconnects

www.ibm.com

Example of interconnect hierarchy



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Interesting Facts (?) and Observations

- **According to Gordon Moore:**
  - There are an estimated 200 million billion transistors in the world!
  - More transistors are manufactured each year than the number of rain drops that fall on California or Ants in the world!
- **According to Vice President Al Gore:**
  - If automobile manufacturing obeyed Moores law, today, our cars would get 100,000 miles per gallon and cost only 50 cents--of course, they would also be less than 1 mm long!